PATENT ABSTRACTS OF JAPAN

(11)Publication number:

62-154029

(43) Date of publication of application: 09.07.1987

(51)Int.Cl.

GO6F 7/52

(21)Application number: 60-292642

(71)Applicant: HITACHI TOBU SEMICONDUCTOR LTD

HITACHI LTD

(22)Date of filing:

27.12.1985

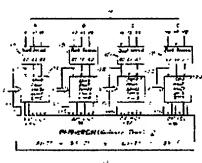
(72)Inventor: SHIMAZU KATSUHIRO **WATANABE KAZUO**

(54) MULTIPLIER CIRCUIT

(57)Abstract:

PURPOSE: To simplify the constitution of a logic circuit obtained a partial product and to speed up remarkably its action by taking a complement of '1' by the algorithm of a booth obtaining a partial product and adding '1' by a Wallence addition tree where a command taking a complement of '2' is given.

CONSTITUTION: Logic operation circuits 2AW2D are constituted so as to take a '1' complement of a multiplicand X if the command taking a '2' complement of the multiplicand X is issued from decoders 1AW1D. If the command taking a '2' complement of the multiplicand X is issued from the decoders 1AW1D, it is directly inputted to an adder circuit 3 as addition data adding one to a complement '1' of the multiplicand X. When a signal C1 becomes active, the corresponding logic operation circuits 2AW2D take the complement of '1' of the multiplicand X, and simultaneously the adder circuit 3 adds outputs (AX', BX', CX' and DX') from the logic operation circuits 2AW2D according to the Wallence tree system. The adder circuit 3 adds one to the output where the signal C1 becomes active.



Ý.

LEGAL STATUS

[Date of request for examination]

Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]